



# PRODUCT/PROCESS CHANGE NOTIFICATION PCN 10986 – Additional information

## ST Shenzhen (China) TSSOP 20 package Back-End line - Additional products

### MDG - Microcontrollers Division (MCD)

#### What are the changes?

	Existing manufacturing site / line		Added manufacturing site / line
Assembly site	Amkor ATP Philippines		ST Shenzhen China
Leadframe (1)	LF FOR TSSOP 20 3X4.2 PPF		LF FOR TSSOP 20 3X4.2 PPF
Resin (2)	SUMITOMO G700K		SUMITOMO G700KC
Glue	GLUE D/A ABLESTIK 8290		GLUE D/A ABLESTIK 8601S25
Wire	Gold 0.8mil		Silver 96.5% 0.8mil
Enhanced Traceability in marking	No digit		2 digits

(1) Lead color and surface finish change depending on leadfinishing.

(2) Package darkness changes depending on molding compound.

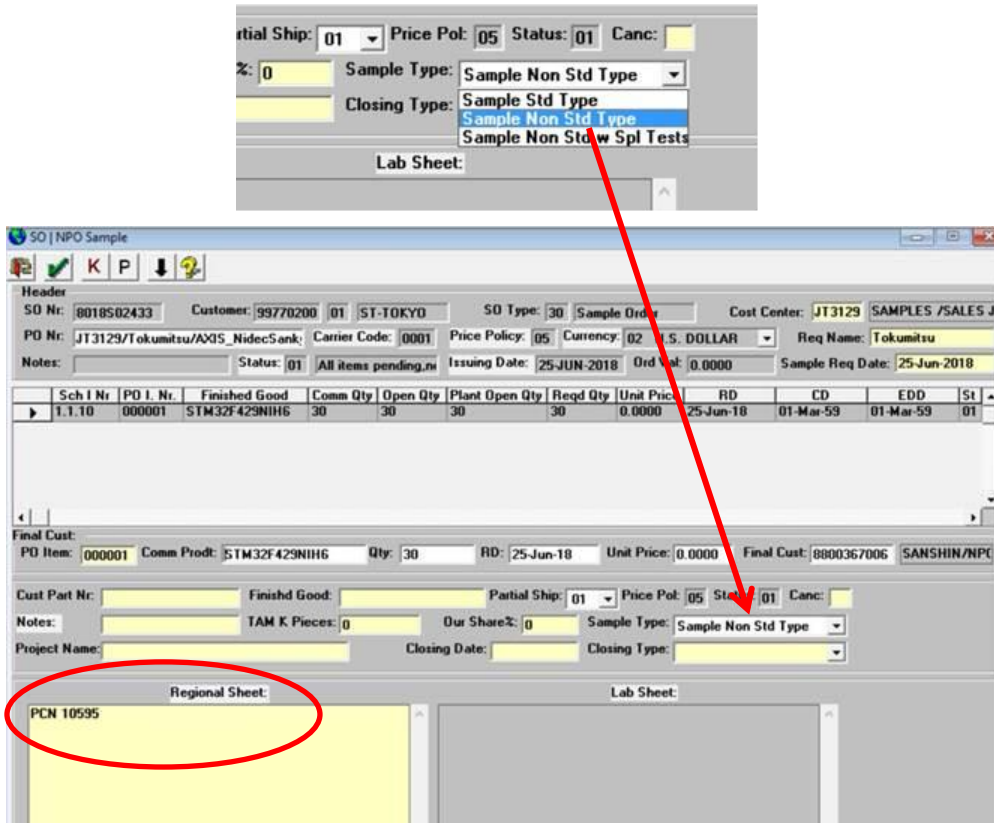
Pin1 identifier can change in terms of form and positioning.

Marking position and size could be different upon assembly site, without any loss of information.

#### How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN10986**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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# MDG- MCD RER1512

## Reliability Report

Qualification Type : ASSEMBLY LINE QUALIFICATION, NEW BILL OF MATERIALS

### TSSOP20 - ST SHENZHEN

### STM8S-STM32 - Dice 767, 444, 758

(PCN MMS-MCD/15/9299 dated 16 Jun 2016)

(PCN MMS-MCD/19/10986 dated 21 Jun 2019)

Product / Process & Package Information	Die 767	Die 444	Die 758
<b>Commercial Product:</b>	STM8S003F3P6	STM32F030F4P6	STM8L051F3P6
<b>Product Line:</b>	STM8S die 767	STM32F die 444	STM8L die 758
<b>Product Description:</b>	Micro 8Bits	Micro 32Bits	Micro 8Bits
<b>Finish Good Code:</b>	IS8S003F3P6\$C3	IS32F030F4P6\$C2	IS8L051F3P6\$C2
<b>Mask Set Revision:</b>	F767XXXY	F444XXXA	F758XXXZ
<b>Silicon Process Technology:</b>	CMOSF9GO1	0.18 Gen.Emb.Flash logic TSMC	CMOSF9GO2
<b>Wafer Fabrication Location:</b>	ST Rousset 8 France	TSMC Fab 8 Taiwan	ST Rousset 8 France
<b>Electrical Wafer Sort Test Plant Location:</b>	ST MICROELECTRONICS Ang Mo Kio EWS Singapore	ARDENTEC  EWS Taiwan	ARDENTEC  EWS Taiwan
<b>Package:</b>	TSSOP 20 BODY 4.4 PITCH 0.65		
<b>Assembly Plant location:</b>	SHENZHEN (China)		
<b>Final Test plant location:</b>	SHENZHEN (China)		

Approval List V1.0			
Function	Location	Name	Date
Division Q&R Responsible	ST Rousset	Gisèle SEUBE	08 Feb 17
Division Quality Manager	ST Rousset	Pascal NARCHE	08 Feb 17

Approval List V2.0			
Function	Location	Name	Date
Division Q&R Responsible	ST Rousset	Gisèle SEUBE	18 jun 19
Division Quality Manager	ST Rousset	Pascal NARCHE	18 jun 19

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# 1 RELIABILITY RESULTS OVERVIEW

## 1.1 Objectives

This report summarizes the reliability results for TSSOP20 2x3.35 package manufactured at ST Shenzhen (China).

Test vehicles are described here below:

Product	Package
STM8S003F3P6	TSSOP 20 BODY 4.4 PITCH 0.65
STM32F030F4P6	TSSOP 20 BODY 4.4 PITCH 0.65
STM8L051F3P6	TSSOP 20 BODY 4.4 PITCH 0.65

## 1.2 Context

Today production is only issued from AMKOR ATP (Philippines). In order to ensure top class service for our customers, given the continued growth of the STM32 & STM8 families, ST Microcontrollers Division will increase production capacity and improve flexibility through the qualification of an additional assembly source.

Changes are described in the below table on TSSOP20:

New Bill of Materials changes are described here below:

Old	New
Current assembly plant : AMKOR ATP (Philippines)  Current Bill Of Materials : - Wire Bonding : 0.8 mil Au - Glue : 8290 Ablestik - Resin : G700K - Leadfinishing : Rough PPF	Current assembly plant, AMKOR ATP (Philippines), remains unchanged.  Additional assembly plant : ST Shenzhen (China)  Additional Bill Of Materials : - Wire Bonding : 0.8 mil Ag - Glue : 8601-S25 Ablestik - Resin : G700KC - Leadfinishing : PPF

(\*) Lead color and surface finish change depending on lead finishing

Changes are qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliance with the JESD-47 international standard.

## 1.3 Conclusion

All reliability tests have been completed with positive results for 767 and 444 dice. Neither functional nor parametric rejects were detected at final electrical testing.

Bond Pad Validation has been completed with positive results for 758 die,

According to the positive Bond Pad Validation and reliability results, the qualification is granted for TSSOP20 at ST Shenzhen.

## 2 RELIABILITY TEST VEHICLES Characteristics

### 2.1 Reliability Test vehicles description

Package line	Assembly Line Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
TSSOP	20L	STM8S (YA*767) STM32 (YA*444) STM8L (YA*758)	F9GO1 TSMC 0.18µm F9GO2	3 3 1 (Bond Pad Validation)

### 2.2 Reliability Information

Lot ID	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7
<b>Die Name /cut:</b>	767			444			758
<b>Diffusion Lot Number:</b>	VG631250	VG631250	VG631250	9U628038	98546004	9U628038	VG848634
<b>Trace Code:</b>	GK6411Y9	GK6411Y9	GK6411Y9	GK6411YA	GK6411YA	GK6411YA	NA
<b>Assy lot number</b>	GK6411Y9RQ	GK6411Y9RJ	GK6411Y9RL	GK6411YARM	GK6411YARK	GK6411YARM	G848634H1
<b>Raw Line Code Package:</b>	C5YA*767ISX Y	C5YA*767ISX Y	C5YA*767ISX Y	C6YA*444ISX 1	C6YA*444ISX 1	C6YA*444ISX 1	C3YA*758ISX Z
<b>Reliability Lab location :</b>	ST Rousset (France)	ST Shenzhen (China)		ST Rousset (France)	ST Shenzhen (China)		

## 2.3 Front-End information

Front-End	767	444	758
<b>Wafer Diameter:</b>	8 inches	8 inches	8 inches
<b>Wafer Thickness:</b>	375 +/-25 $\mu\text{m}$	381 +/-25 $\mu\text{m}$	375 +/-25 $\mu\text{m}$
<b>Die Size:</b>	1.334 X 2.210 $\mu\text{m}$	2.458 X 2.360 $\mu\text{m}$	1.562 X 2.238 $\mu\text{m}$
<b>Scribe Line size x/y:</b>	80 X 80 $\mu\text{m}$	80 X 80 $\mu\text{m}$	80 X 80 $\mu\text{m}$
<b>Pad Die Size /Pad type:</b>	65 X 108 $\mu\text{m}$	65 X 70 $\mu\text{m}$	65 X 108 $\mu\text{m}$
<b>Metal Layers Number /Materials /Thickness:</b>	Metal 1 TaN/Ta/Cu 0.280 $\mu\text{m}$ Metal 2 TaN/Ta/Cu 0.350 $\mu\text{m}$ Metal 3 TaN/Ta/Cu 0.350 $\mu\text{m}$ Metal 4 Ti/AlCu/TxTN 0.900 $\mu\text{m}$	Metal 1 Tin/AlCu/Tin 0.450 $\mu\text{m}$ Metal 2 Tin/AlCu/Tin 0.450 $\mu\text{m}$ Metal 3 Tin/AlCu/Tin 0.450 $\mu\text{m}$ Metal 4 Tin/AlCu/Tin 0.450 $\mu\text{m}$ Metal 5 Tin/AlCu/Tin 0.875 $\mu\text{m}$	Metal 1 TaN/Ta/Cu 0.280 $\mu\text{m}$ Metal 2 TaN/Ta/Cu 0.350 $\mu\text{m}$ Metal 3 TaN/Ta/Cu 0.350 $\mu\text{m}$ Metal 4 TaN/Ta/Cu 0.350 $\mu\text{m}$ Metal 5 Ti/AlCu/TxTN 0.900 $\mu\text{m}$
<b>Passivation Layers Thickness:</b>	USG + NitUV (HFP USG+UV Nitride)	HDPox 10kA+SRO 1.5kA+PESIN 6kA	USG + NitUV (HFP USG+UV Nitride)
<b>Back Metal Finishing</b>	RAW SILICON - BACK GRINDING	RAW SILICON - BACK GRINDING	RAW SILICON - BACK GRINDING

## 2.4 Back-End information

Back-End	767	444	758
<b>Assembly Plant Location/ Address:</b>	Shenzen STS Microelectronics co.,Ltd 16, Tao Hua Rd. Futian Free Trade Zone Shenzhen, P.R. China 518048	Shenzen STS Microelectronics co.,Ltd 16, Tao Hua Rd. Futian Free Trade Zone Shenzhen, P.R. China 518048	Shenzen STS Microelectronics co.,Ltd 16, Tao Hua Rd. Futian Free Trade Zone Shenzhen, P.R. China 518048
<b>Die Thickness after Back grinding:</b>	280 μm +/-20μm	280 μm +/-20μm	280 μm +/-20μm
<b>Die sawing method:</b>	Step cut	Step cut	Step cut
<b>Die attach material:</b>	Glue 8601S-25	Glue 8601S-25	Glue 8601S-25
<b>Type:</b>	Loctite	Loctite	Loctite
<b>Supplier:</b>	Ablestik Henkel	Ablestik Henkel	Ablestik Henkel
<b>Lead frame material:</b>	TSSOP 20L COPER HDMt OpA C7025	TSSOP 20L COPER HDMt OpB C7025	TSSOP 20L COPER HDMt OpA C7025
<b>L/F Finishing Type:</b>	NiPdAu	NiPdAu	NiPdAu
<b>Die paddle size:</b>	2x3.35	2x4.20	3x4.20
<b>Supplier:</b>	ASM	ASM	ASM
<b>Wire bonding:</b>	AG 96,5% WIRE	AG 96,5% WIRE	AG 96,5% WIRE
<b>Type /Diameter:</b>	0.8MIL	0.8MIL	0.8MIL
<b>Supplier:</b>	MKE	MKE	MKE
<b>Pitch:</b>	80μm	80μm	80μm
<b>POA:</b>	0087225	0087225	0087225
<b>Molding Compound Supplier:</b>	EME-G700KC SUMITOMO	EME-G700KC SUMITOMO	EME-G700KC SUMITOMO
<b>Package Moisture Sensitivity Level (JEDEC J-STD020D):</b>	1	1	1



### 3 RELIABILITY RESULTS SUMMARY

#### 3.1 Die oriented test

Description	Die Related Tests					Results TSSOP20	
	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	767	444
						Lot1	Lot4
<i>Electrostatic discharge – Charge Device Model</i>							
ESD CDM	ANSI/ESD STM5.3.1	500V 1KV	3 units	500V for dice 444 1KV for 767	NA	0/3	0/3

#### 3.2 Package Oriented Test

Description	Package Related Tests					Results TSSOP20					
	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	767			444		
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6
<i>Preconditioning: moisture sensitivity level 1</i>											
PC	J-STD-020 JESD22-A113	MSL1	241 units	Electrical test: A0/R1 (Accepted 0 reject/ Rejected 1 reject)	NA	0/231	0/231	0/231	0/231	0/231	0/231
		Delamination				0/60	0/231	0/231	0/60	0/231	0/231
<i>High Temperature Storage Life (No preconditioning)</i>											
HTSL	JESD 22-A103	150°C	77 units	Elect test A0/R1	1000h	0/77	0/77	0/77	0/77	0/77	0/77
<i>Thermal Cycling after Preconditioning</i>											
TC	JESD 22-A104	-65c/+150°c	77 units	Elect test A0/R1	500cy	0/77	0/77	0/77	0/77	0/77	0/77
					1000cy	0/77	0/77	0/77	0/77	0/77	0/77
<i>Wire Bond Shear after Thermal Cycling</i>											
Wire Bond Shear	AEC Q100-001	Min bond shear 15g after TC	10 wires x 3 units	A0/R1	After TC 500cy TC 1000cy	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30
<i>Wire Bond Pull after Thermal Cycling</i>											
Wire Bond Pull	Mil Std 883 Method 2011	Minimum pull strength after TC=3 grams after TC	10 wires x 3 units	A0/R1	After TC 500cy TC 1000cy	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30	0/30 0/30



Autoclave / Unbiased Highly Accelerated Temperature and Humidity Stress after Preconditioning											
AC	JESD 22A102	121°C ,100% 2Atm RH	77 units	Elect test A0/R1	96h 192h		0/77 0/77	0/77 0/77		0/77 0/77	0/77 0/77
UHASt	JESD 22 A118	130°C ,85% 2Atm RH	77 units	Elect test A0/R1	96h	0/77			0/77		
Temperature Humidity Bias / Storage after Preconditioning											
THB	JESD 22A101	85°C/85%RH Bias	77 units	Elect test A0/R1	1000h		0/77	0/77		0/77	0/77
THS	JESD 22A118	85°C/85%RH UnBias	77 units	Elect test A0/R1	1000h	0/77			0/77		
Construction Analysis											
CA	Construction Analysis including : -Wire bond shear -Wire bond pull -Solderability -Physical Dimension	JESD 22B102 JESDB100/ JESDB108	50			No concern	No concern			No concern	

## 4 APPLICABLE AND REFERENCE DOCUMENTS

<b>ADCS/DMS 0061692 :</b>	Reliability Tests And Criteria For Qualifications
<b>SOP 2.6.2:</b>	Process qualification and transfer management
<b>SOP 2.6.7:</b>	Product Maturity Level
<b>SOP 2.6.9:</b>	Package and process maturity management in Back End
<b>SOP 2.6.11:</b>	Program management from product qualification
<b>SOP 2.6.19:</b>	Process maturity level
<b>ANSI-ESD STM5.3.1:</b>	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
<b>JESD 22-A103</b>	High Temperature Storage Life
<b>J-STD-020D:</b>	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
<b>JESD22-A113:</b>	Preconditioning of non-hermetic surface mount devices prior to reliability testing
<b>JESD22-A102:</b>	Autoclave test (pressure pot)
<b>JESD22-A118:</b>	Unbiased Highly Accelerated Temperature and Humidity Stress Temperature Humidity Storage – No Bias (ST customize)
<b>JESD22-A104:</b>	Temperature cycling
<b>JESD22-A101:</b>	Temperature Humidity Bake
<b>JESD 22B102:</b>	Solderability test
<b>JESD22B100/B108:</b>	Physical dimension

## 5 GLOSSARY AND TESTS DESCRIPTION

<b>PC</b>	Preconditioning (solder simulation)
<b>THB</b>	Temperature Humidity Bias
<b>THS</b>	Temperature Humidity Storage – No Bias
<b>TC</b>	Temperature cycling
<b>AC</b>	Autoclave test (pressure pot)
<b>UHASt</b>	Unbiased Highly Accelerated Temperature and Humidity Stress
<b>HTSL</b>	High temperature storage life
<b>ADCS/DMS</b>	ST Advanced Documentation Controlled system/ Documentation Management system
<b>ESD CDM</b>	Electrostatic discharge (charge device model)
<b>CA</b>	Construction Analysis

## 6 REVISION HISTORY

Version	Date	Author	Comment
1.0	18 Feb 17	Cedric CHASTANG	Initial release for qualification
2.0	18 Jun 19	Cedric CHASTANG	Qualification of F9G02 devices by Bond Pad Validation

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